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	SPECIFICATION	

DEVICE SPECIFICATION for

Passive Matrix COLOR LCD Module

(640x480 dots)

Model No.

LM64C27P

❑ ICUSTOMER'S APPROVAL"

DATE

BY

PRESENTED

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LIQUID CRYSTAL DISPLAY GROUP

SHARP CORPORATION

SHARP

SPEC No.	MODEL No.
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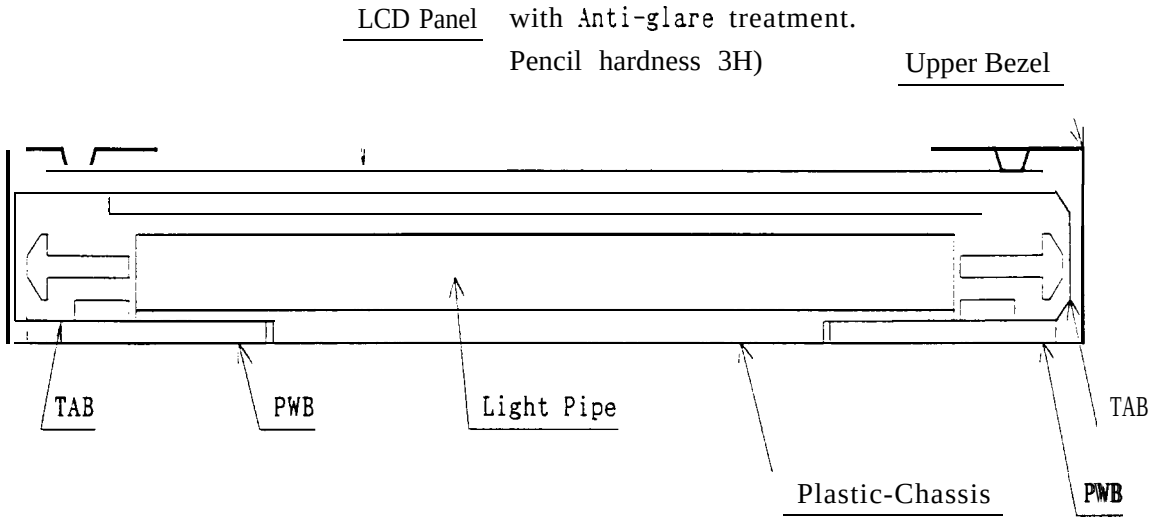
1. Application

   This data sheet is to ntroduce the specification of LM64C26P,Passive Matr x type Color LCD Module.

2. Construction and Outline

   Construction: 640x480 dots color display module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TAB(tape automated bonding) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.
   Signal ground(VSS) is connected with the metal bezel.
   DC/DC converter is built in.



Outline : See Fig. 10
Connection : See Fig. 10 and Table 6

3. Mechanical Specifications

Table 1

	Parameter	Specifications	Unit
	Outline dimensions	221.0 (W) X156.0 (H) X8.2 MAX(D)	mm
	Active area	170.855 (W) X128.135(H)	mm
⚠	Viewing area	175.4(W) X132.7(H)	
	Display format	640(W) X480(H) full dots	−
	Dot size	0.089 xRGB(W) X0.267(H)	mm
	Dot spacing	0.025	mm
	*1 Base color	Normally black *2	−
	Weight	Approx. 310	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display
Display data "H" : ON + transmission
Display data "L" : OFF → light isolation

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbo 1	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	v	Ta=25 "C
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	v	Ta=25 "C

4-2 Environments Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 "C	+60 "C	O ℃	+40 ℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z)
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40 "C . . . ..95 %RHMax

Ta>40 ℃. . . ..Absolute humidity shall be less than Ta=40 "C/95 %RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	—	9.8 m/s²
Vibration width	0.075 mm	—
Interval	10 Hz～500 H,-10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X/±Y/±Z

Note 4) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

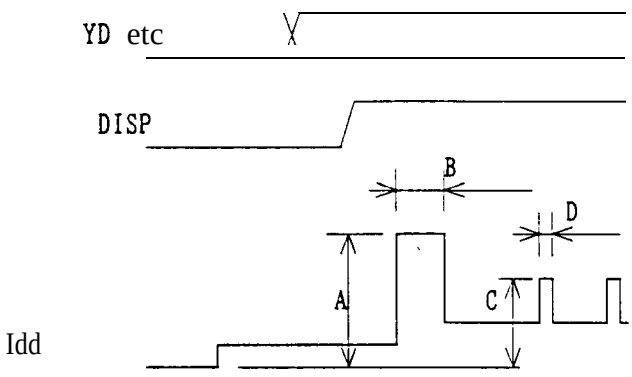
Table 5 Ta=25 ℃, V_{DD}=3.3 V±0.3V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Ta=0~40℃	3.0	3.3	3.6	v
Contrast adjust voltage	Vcon -Vss	Ta=O "C	0.8	–	–	V
		Ta=25 ℃	1.35	1.95	2.55	V
		Ta=40 ℃			2.80	
Input signal voltage	V_{IN}	*H" level	0.8V_{DD}	–	V_{DD}+0.3	v
		"L" level	-0.3	–	0.2V_{DD}	v
Input leakage current	I_{ILL} (Logic)	"H" level	–	–	1.0	μA
		"L" level	-1.0	–	–	
	I_{ILV}	Vcont=2.8V	-1.0	–	1.0	mA
Supply current(Logic)	I_{DD}	Note 2)	–	180	270	mA
Power consumption	Pd	Note 2)		600	900	mW
Rush Current (Logic)	I_{DD}	Ta=25 ℃, Note1)-①	-	-	2 A × 5 ms	
		Ta=25 ℃, Note1)-②	–	–	1 A × 0.6 ms	

Note 1) Under the following conditions. ;Logic voltage(V_{DD}) should be designed to supply following Inrush current.

①Immediately after the rise of DISP signal.

②Under the situation that DISP signal is on and kept steady.



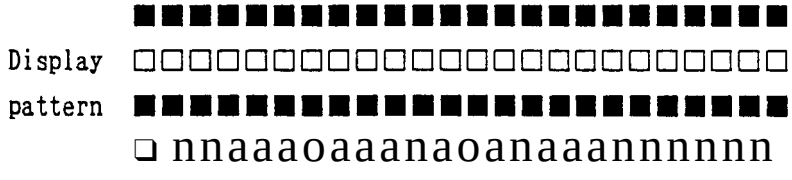
Measurement Curcuit:TMD-18-3
(Vdd Power Supply) (TAKASAGO)

A: 2 A MAX
B: 5 ms MAX
C: 1 A MAX
D: 0.6 ms MAX

Note 2) Under the following conditions. ;

Vcon-Vss : contrast ❑ ax.(1.95 V TYP)

V_{DD}-Vss=3.3 V, Frame frequency=73 Hz, Display pattern = black/white stripe pattern.



❑ nnaaaoaaanaoanaaannnnnn

This value is direct current.

5-3 Interface signals

OLCD

Table 6

Pin No	Symbol	Description	Level
1	DUO	Display data signal (Upper)	H(ON), L(OFF)
2	V_{SS}	Ground potential	—
3	DU1	Display data signal (Upper)	H(ON), L(OFF)
4	YD	Scan start-up signal	"H"
5	DU2	Display data signal (Upper)	H(ON), L(OFF)
6	LP	Input data latch signal	"H"→"L"
7	DU3	Display data signal (Upper)	H(ON), L(OFF)
8	V_{SS}	Ground potential	—
9	V_{SS}	Ground potential	
10	XCK	Data input clock signal	"H"→"L"
11	DL4	Display data signal (Lower)	H(ON), L(OFF)
12	V_{CON}	Contrast adjust voltage	—
13	DL5	Display data signal (Lower)	H(ON), L(OFF)
14	V_{DD}	Power supply for logic and LCD(3.3 V)	—
15	V_{SS}	Ground potential	—
16	V_{DD}	Power supply for logic and LCD(3.3 V)	—
17	DL6	Display data signal (Lower)	H(ON), L(OFF)
18	DISP	Display control signal	H(ON), L(OFF)
19	DL7	Display data signal (Lower)	H(ON), L(OFF)
20	NC		—
21	V_{SS}	Ground potential	—
22	DU7	Display data signal (Upper)	H(ON), L(OFF)
23	DLO	Display data signal (Lower)	H(ON), L(OFF)
24	DU6	Display data signal (Upper)	H(ON), L(OFF)
25	DL1	Display data signal (Lower)	H(ON), L(OFF)
26	DU5	Display data signal (Upper)	H(ON), L(OFF)
27	V_{SS}	Ground potential	—
28	DU4	Display data signal (Upper)	H(ON), L(OFF)
29	DL2	Display data signal (Lower)	H(ON), L(OFF)
30	V_{SS}	Ground potential	—
31	DL3	Display data signal (Lower)	H(ON), L(OFF)

○CCFT

Pin No	Symbo 1	Description	Leve l
1	HV	High voltage lineal (from Inverter)	
2	NC		—
3	GND	Ground line (from Inverter)	—

NOTE) Pin No. and its location are shown in Fig.10.

OLCD

Used connector:DF9B-31P-1V (HIROSE)

Mating connector:DF9B-31S-1V (HIROSE)

○CCFT

Used connector:BHR-03VS-1 (JST)

Mating connector: SM03(4.O) B-BHS or SM02(8.O) B-BHS(JST)

Except above connector shall be out of guaranty

5-3 Interface signals

OLCD

Table 6

Pin No	Symbol	Description	Level
1	DUO	Display data signal (Upper)	H(ON), L(OFF)
2	V_{SS}	Ground potential	—
3	DU1	Display data signal (Upper)	H(ON), L(OFF)
4	YD	Scan start-up signal	"H"
5	DU2	Display data signal (Upper)	H(ON), L(OFF)
6	LP	Input data latch signal	"H"→"L"
7	DU3	Display data signal (Upper)	H(ON), L(OFF)
8	V_{SS}	Ground potential	—
9	V_{SS}	Ground potential	
10	XCK	Data input clock signal	"H"→"L"
11	DL4	Display data signal (Lower)	H(ON), L(OFF)
12	V_{CON}	Contrast adjust voltage	—
13	DL5	Display data signal (Lower)	H(ON), L(OFF)
14	V_{DD}	Power supply for logic and LCD(3.3 V)	—
15	V_{SS}	Ground potential	—
16	V_{DD}	Power supply for logic and LCD(3.3 V)	—
17	DL6	Display data signal (Lower)	H(ON), L(OFF)
18	DISP	Display control signal	H(ON), L(OFF)
19	DL7	Display data signal (Lower)	H(ON), L(OFF)
20	NC		—
21	V_{SS}	Ground potential	—
22	DU7	Display data signal (Upper)	H(ON), L(OFF)
23	DLO	Display data signal (Lower)	H(ON), L(OFF)
24	DU6	Display data signal (Upper)	H(ON), L(OFF)
25	DL1	Display data signal (Lower)	H(ON), L(OFF)
26	DU5	Display data signal (Upper)	H(ON), L(OFF)
27	V_{SS}	Ground potential	—
28	DU4	Display data signal (Upper)	H(ON), L(OFF)
29	DL2	Display data signal (Lower)	H(ON), L(OFF)
30	V_{SS}	Ground potential	—
31	DL3	Display data signal (Lower)	H(ON), L(OFF)

○CCFT

Pin No	Symbo 1	Description	Leve l
1	HV	High voltage lineal (from Inverter)	
2	NC		—
3	GND	Ground line (from Inverter)	—

NOTE) Pin No. and its location are shown in Fig.10.

OLCD

Used connector:DF9B-31P-1V (HIROSE)

Mating connector:DF9B-31S-1V (HIROSE)

○CCFT

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Except above connector shall be out of guaranty

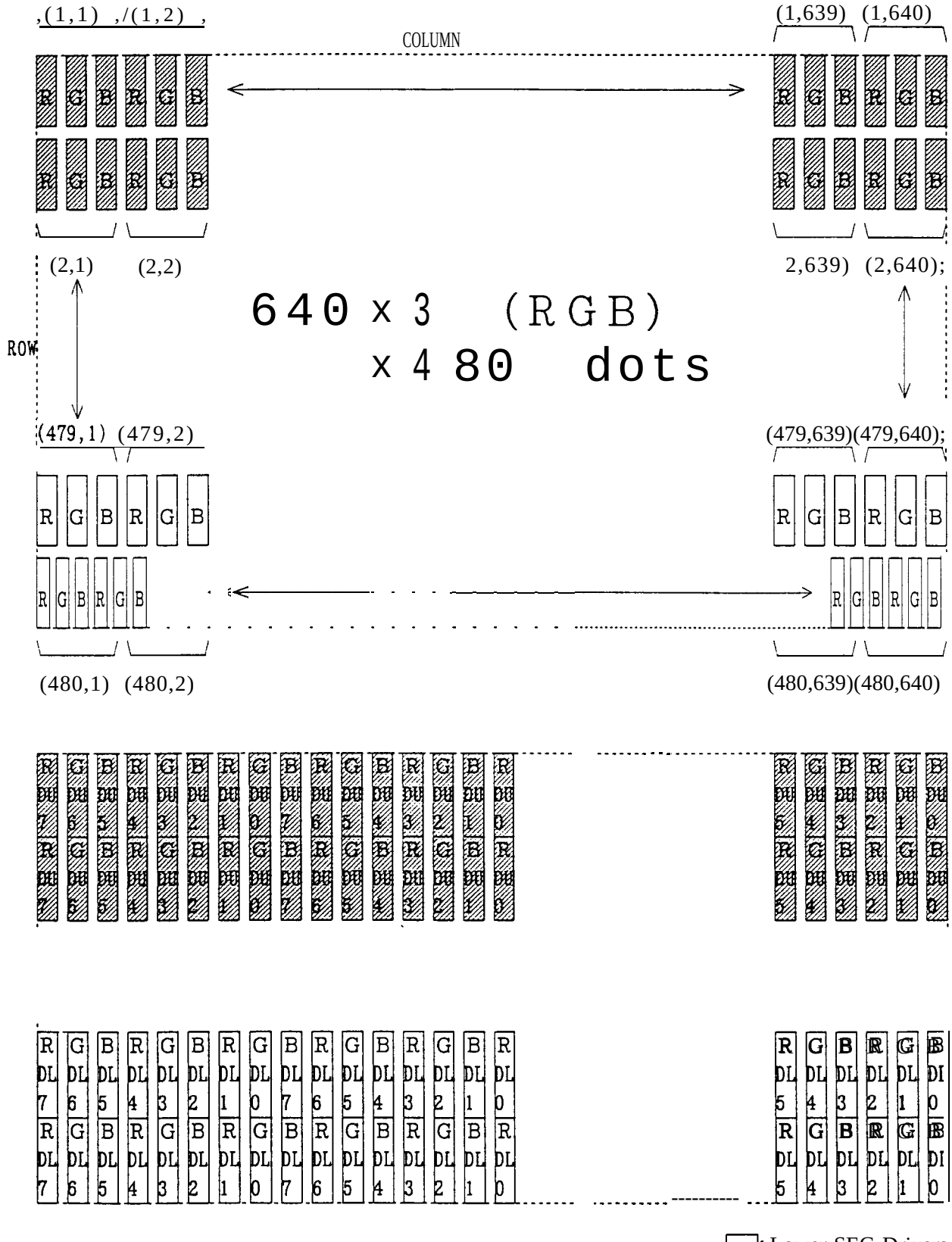
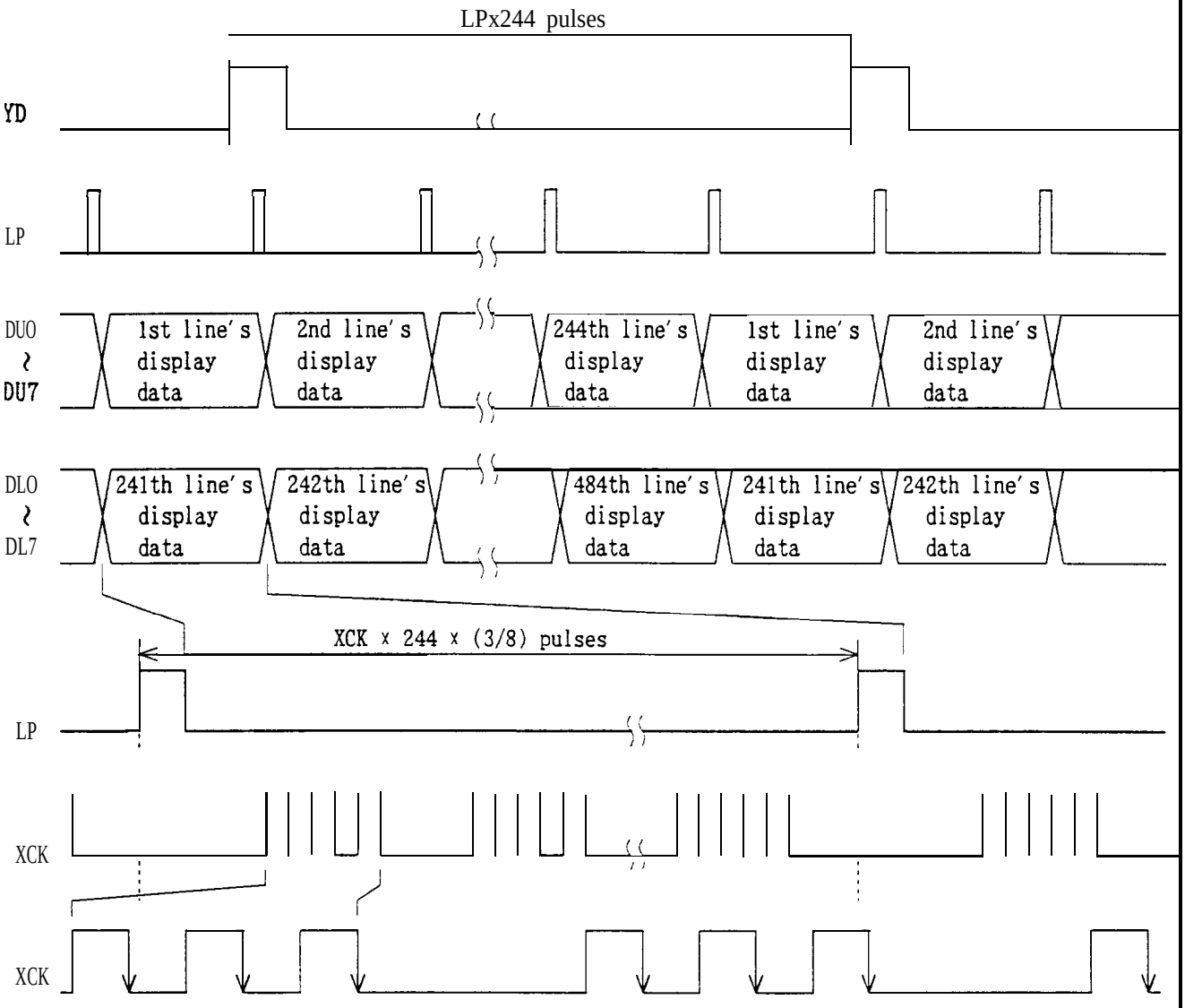


Fig.1 Dot chart of display area



DU7	R(1,1)	B(1,3)	G(1,6)				R(1,9)	B(1,11)	G(1,14)				
DU6	G(1,1)	R(1,4)	B(1,6)				G(1,9)	R(1,12)	B(1,14)				
DU5	B(1,1)	G(1,4)	R(1,7)				B(1,9)	G(1,12)	R(1,15)				
DU4	R(1,2)	B(1,4)	G(1,7)				R(1,1O)	B(1,12)	G(1,15)				
DU3	G(1,2)	R(1,5)	B(1,7)				G(I,1O)	R(1,13)	B(1,15)				
DU2	B(1,2)	G(1,5)	R(1,8)				B(1,1O)	G(1,13)	R(1,16)				
DU1	R(1,3)	B(1,5)	G(1,8)				R(1,11)	B(1,13)	G(1,16)				
DU0	G(1,3)	R(1,6)	B(1,8)				G(1,11)	R(1,14)	B(1,16)				

DL7	R(241,1)	B(241,3)	G(241,6)				R(241,9)	B(241,11)	G(241,14)				
DL6	G(241,1)	R(241,4)	B(241,6)				G(241,9)	R(241,12)	B(241,14)				
DL5	B(241,1)	G(241,4)	R(241,7)				B(241,9)	G(241,12)	R(241,15)				
DL4	R(241,2)	B(241,4)	G(241,7)				R(241,1O)	B(241,12)	G(241,15)				
DL3	G(241,2)	R(241,5)	B(241,7)				G(241,1O)	R(241,13)	B(241,15)				
DL2	B(241,2)	G(241,5)	R(241,8)				B(241,10)	G(241,13)	R(241,16)				
DL1	R(241,3)	B(241,5)	G(241,8)				R(241,11)	B(241,13)	G(241,16)				
DLO	G(241,3)	R(241,6)	B(241,8)				G(241,11)	R(241,14)	B(241,16)				

Fig.2 Data input timing chart

Table. 7 Interface timing ratings(Ta=0～40 "C, VDD=3.3 V±0.3 V)

Item	Symbol	Rating			Unit
		MIN.	TYP .	MAX.	
Frame cycle *1	tFRM	7.69		16.94	ms
YD signal "H" level set up time	tHYs	100			ns
"H" level hold time	tHYH	100			ns
"L" level set up time	tLYS	100			ns
"L" level hold time	tLYH	100			ns
LP signal "H" level pulse width	tWLPH	350			ns
LP signal clock cycle *3	tLP	10		70	us
XCK signal clock cycle	tCK	82			ns
'H" level clock width	tWCKH	30			ns
"L" level clock width	tWCKL	30			ns
Data set up time	tDS	25			ns
hold time	tDH	30			ns
LP↑ allowance time from XCK↓	tLS	200			ns
XCK↑ allowance time from LP↓	tLH	200			ns
Input signal rise/fall time *2	tr,tf			20	ns

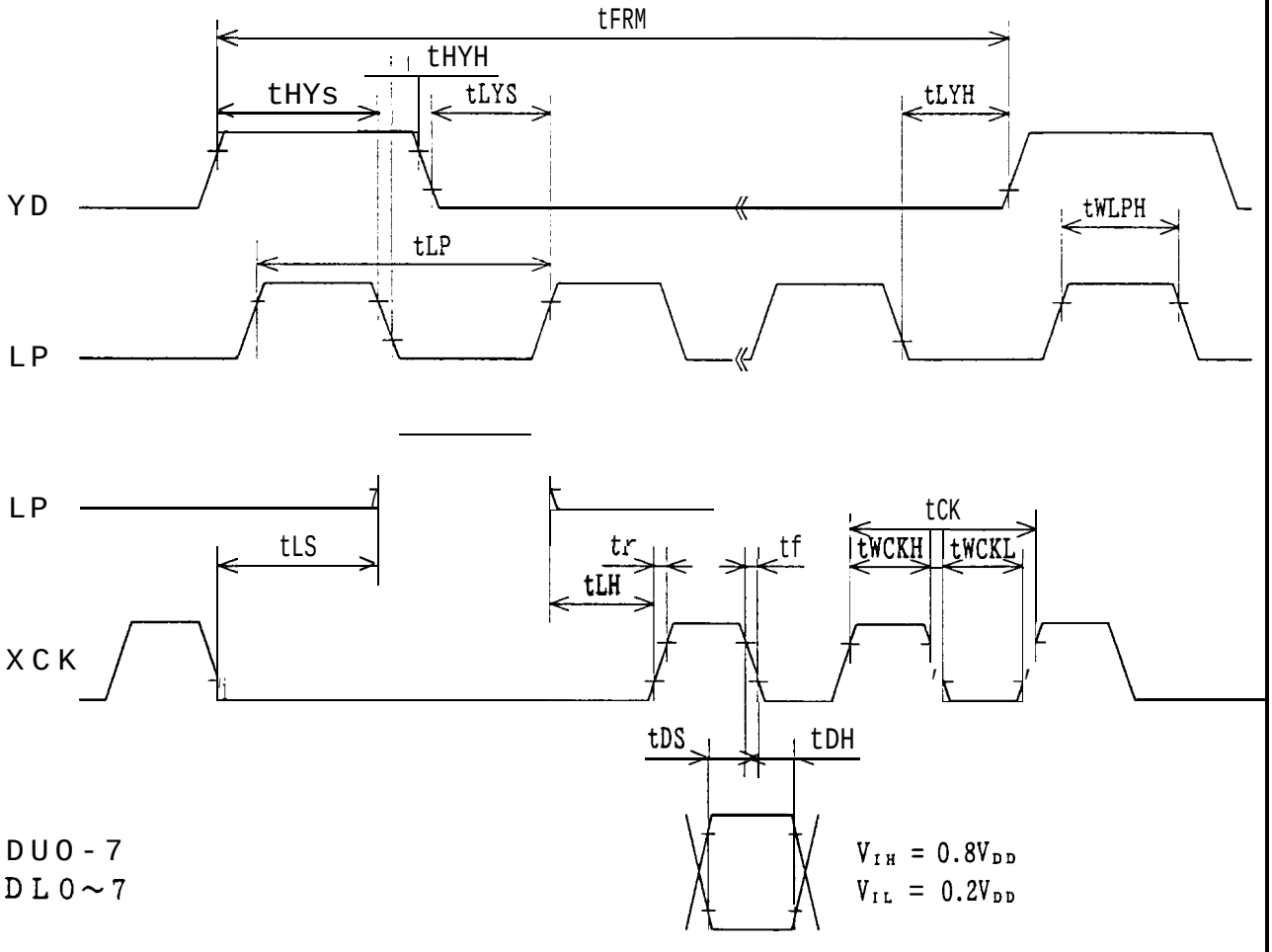


Fig. 3 Interface timing chart

*1 LCD unit functions at the minimum frme cycle of 7.69 ms(Maximum frame frequency of 130 Hz) .
Owing to the characteristics of LCD unit, "shadowing" will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments,frame cycle of 12.8 ms Min. or frame frequency of 78 Hz Max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgement of display quality is subjective and display quality such as "shadowing" is patturn dependent,it is recommended that decision of frame frequency, to which power consumption of the LCD unit is propotional,be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2 \geqq 10$ ns ... 10 ns MAX
$(t_{CK}-t_{WCKH}-t_{WCKL})/2 < 10$ ns ... $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ MAX

*3 The intervals of 1 LP fall and the next must be always the same when the LCD UNIT is active driving.
AndLP's must be input continuously.

6. Module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the module's circuitry.

6.2 Display Face Configuration

The display consists of 640x3(R,G,B)x480 dots as shown in Fig.1.
The interface is single panel with double drive to be driven at 1/244 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (640x3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal (XCK).

When input of one row (640 x 3,R,G,B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 640 x 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640x3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.
Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers. Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DU0～7 and DL0～7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requ res the above data and timing pulse inputs even for static display.

The tim ng chart of input signals are shown in Fig. 3 and Table 7.

7.Optical Characteristics

Ta= 25 ℃, V_{DD} = 3.3 V, Vcon-V_{ss} =Vmax

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0°$) will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co>5.0	$\theta y=0°$	-30	-	30	dgr.	Note1)
		θy		$\theta x=0°$	-15	·	25	dgr.	
Contrast ratio		Co	$\theta x=\theta y=0°$		-	25	-		Note2)
Response time	Rise	τr	$\theta x=\theta y=0°$		-	230	300	ms	Note3)
	Decay	τd	$\theta x=\theta y=0°$		-	80	110	ms	
Unit chromaticity	White	x	$\theta x=\theta y=0°$		-	0.248	-	-	
		y	$\theta x=\theta y=0°$		-	0.329	-	-	

Note 1) The viewing angle range is defined as shown Fig.4.

Note 2) Contrast ratio is defined as follows:

$$Co=\frac{\text{Luminance(brightness) all pixels “White” at Vmax}}{\text{Luminance(brightness) all pixels “dark “ at Vmax}}$$

Vmax is defined in Fig.6.

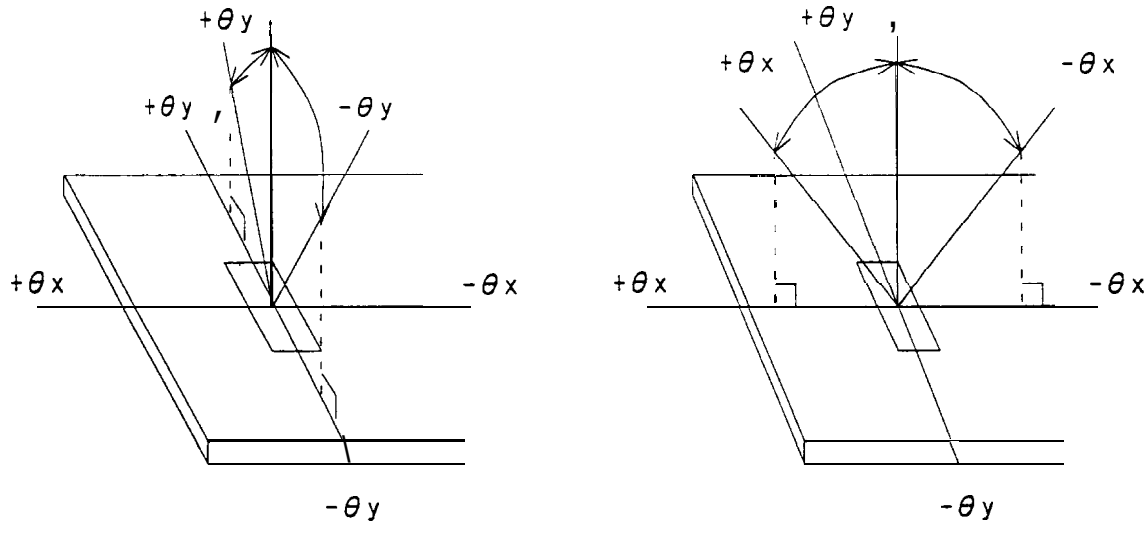
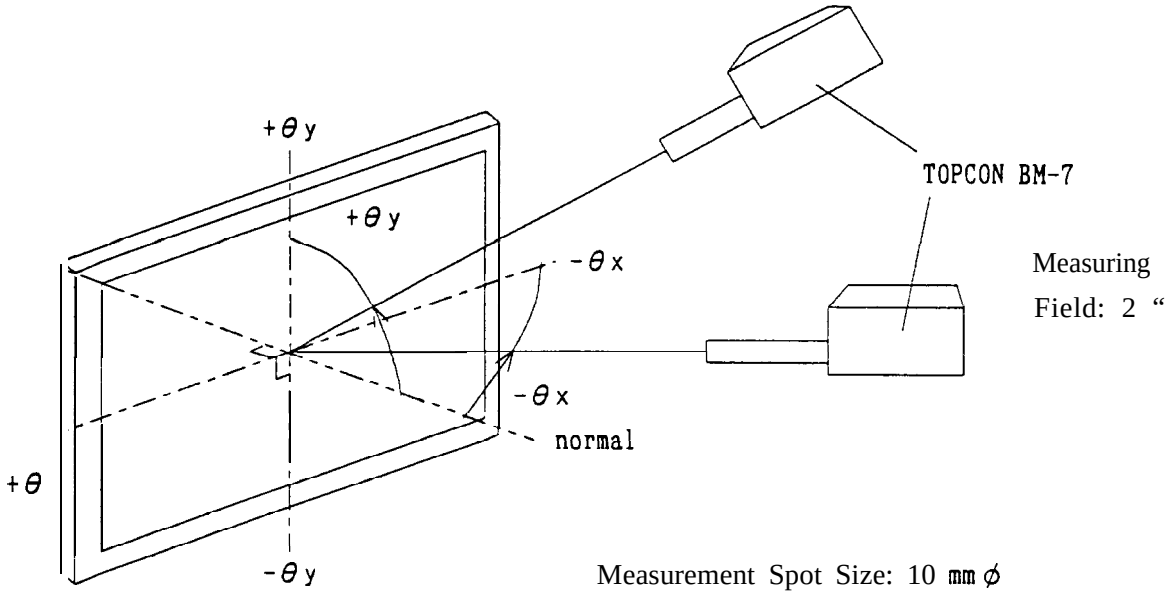


Fig.4 Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.7,assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig.8.



Measurement Spot Size: 10 mm ϕ

θx:Angle from “normal” to viewing surface roteted about the horizontal axis.

θy:Angle from “normal” to viewing surface roteted about the vertical axis.

Fig. 5 Optical Characteristics ‘Test Method I

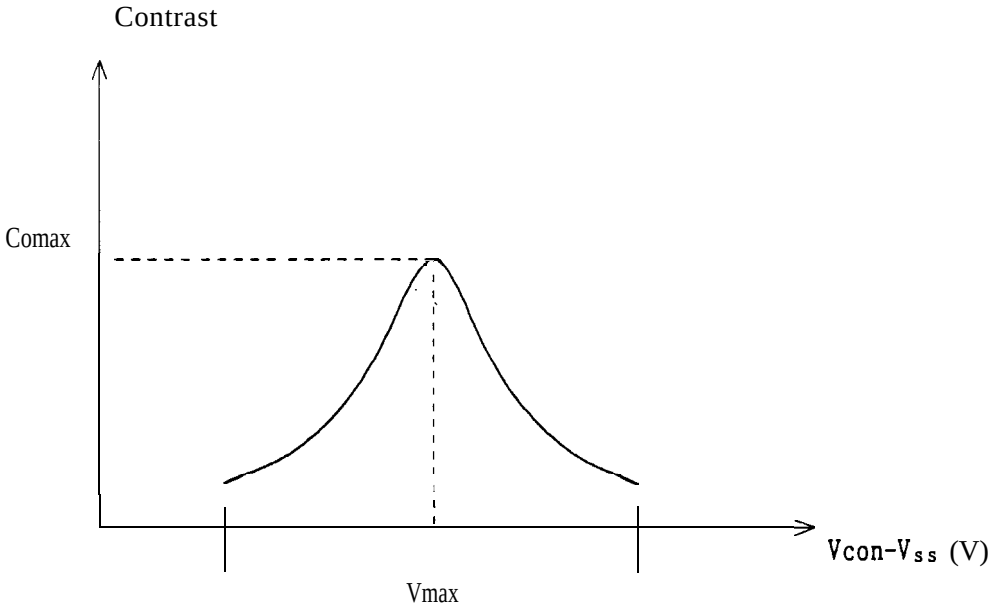


Fig. 6 Definition of V_{Max}

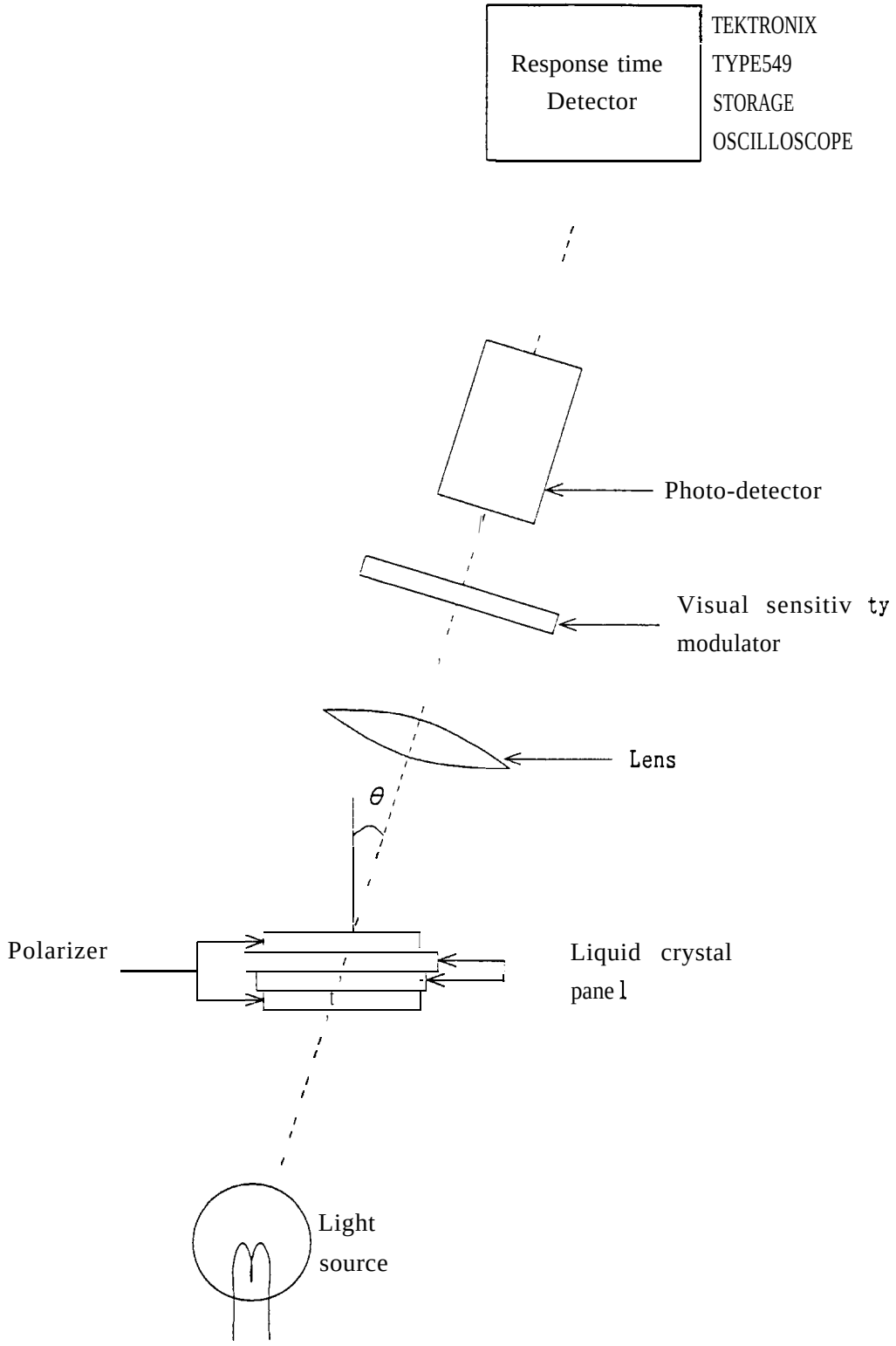
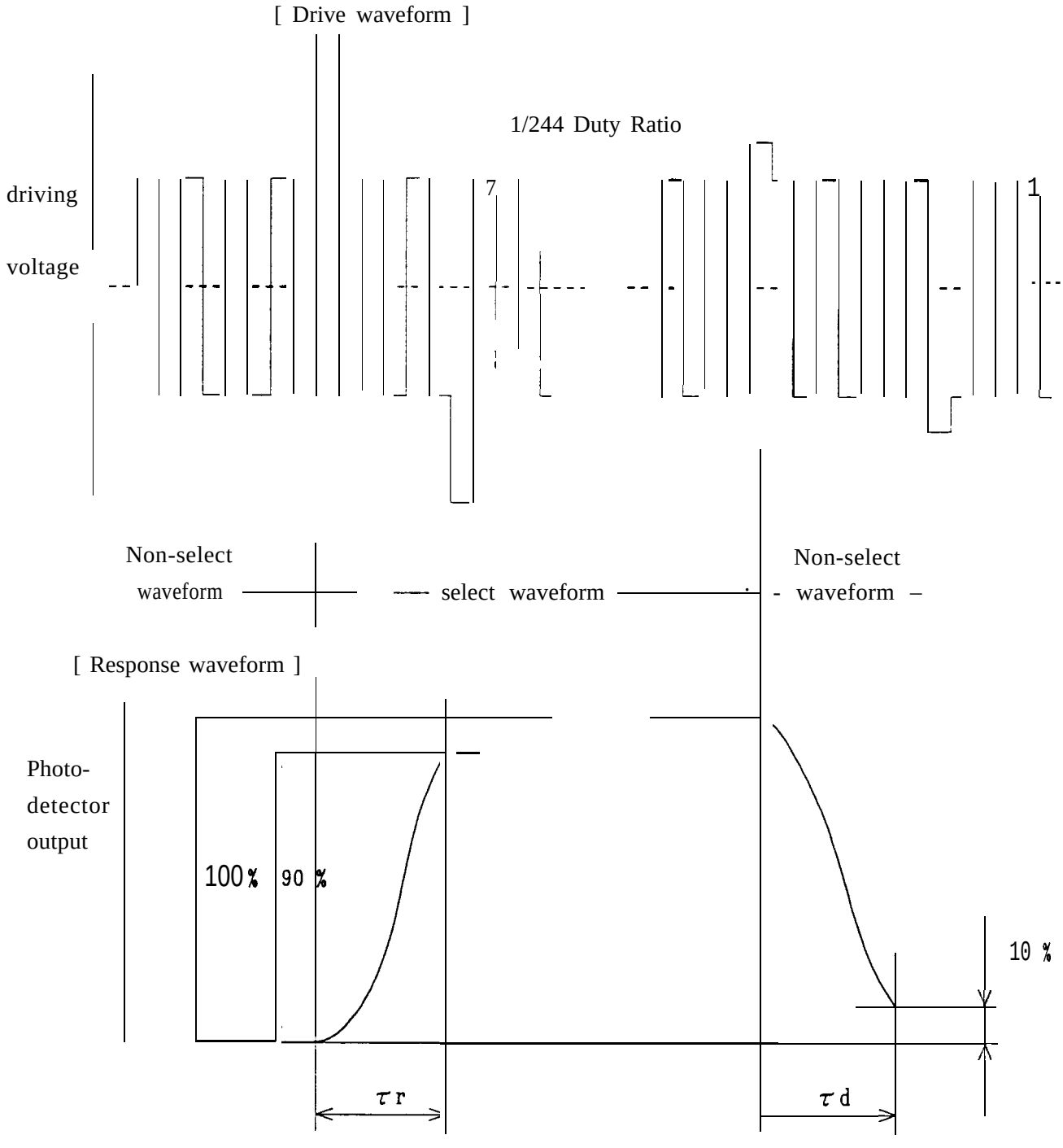


Fig.7 Optical Characteristics Test Method II



τr: Rise time

τd: Decay time

Fig.8 Definition of Response Time

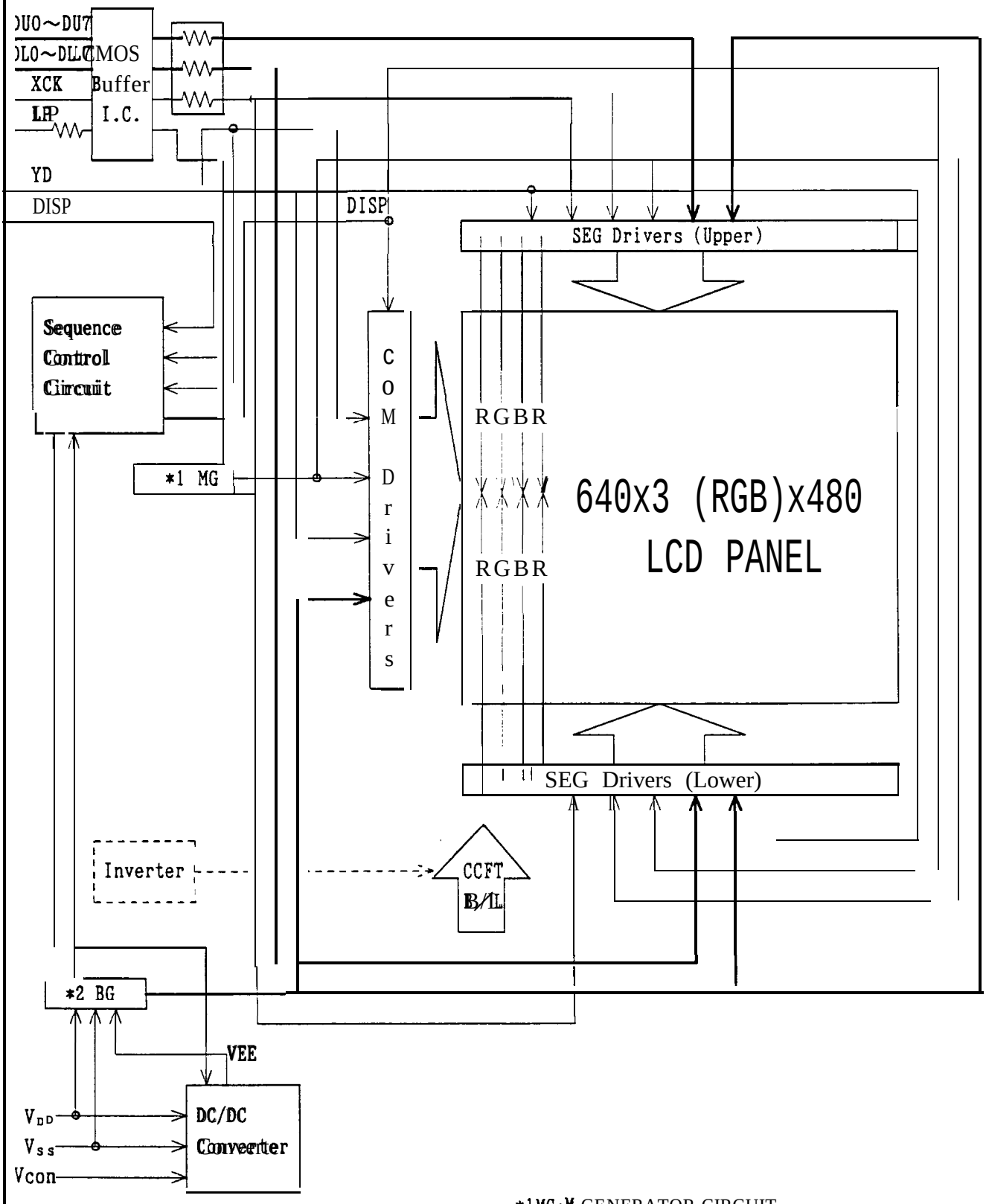


Fig.9 Circuit block diagram

*1MG:M GENERATOR CIRCUIT

*2BG:BIAS GENERATOR & PROTECTION CIRCUIT

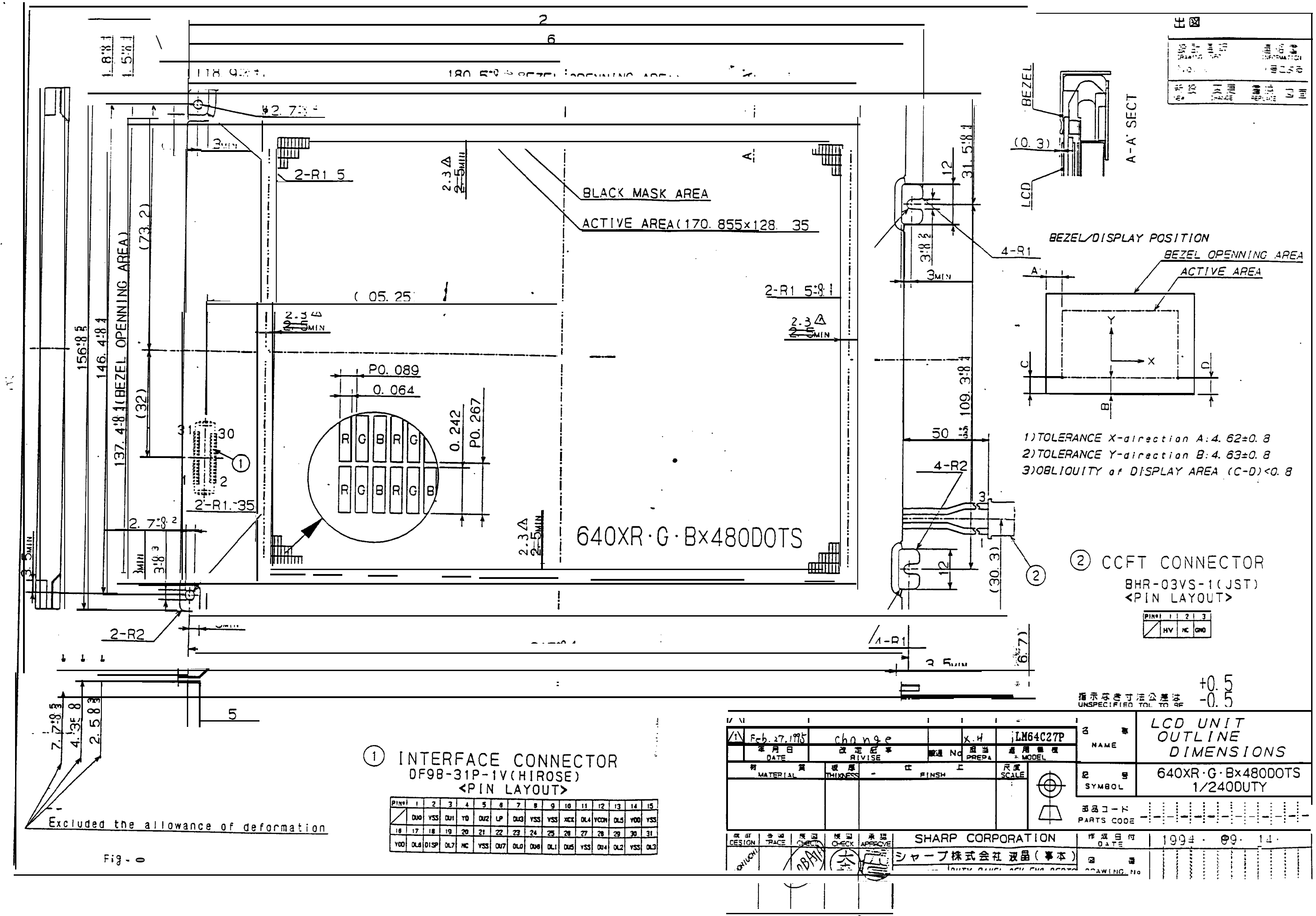


Fig-0

① INTERFACE CONNECTOR

DF9B-31P-1V(HIROSE)

<PIN LAYOUT>

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	DU0	VSS	DU1	Y0	DU2	LP	DU3	VSS	VSS	XCK	DU4	YCOM	DU5	YDD	VSS
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
YDD	DU6	DISP	DU7	NC	VSS	DU7	DU0	DU6	DU1	DU5	VSS	DU4	DU2	VSS	DU3

② CCFT CONNECTOR

BHR-03VS-1(JST)

<PIN LAYOUT>

Pin	1	2	3
	HV	NC	GND

BEZEL
(0.3)
LCD
A-A' SECT

BEZEL/DISPLAY POSITION

BEZEL OPENNING AREA
ACTIVE AREA

1) TOLERANCE X-direction A: 4.62±0.8
2) TOLERANCE Y-direction B: 4.63±0.8
3) OBLIQUITY of DISPLAY AREA (C-D)<0.8

指示なき寸法公差は UNSPECIFIED TOL TO BE +0.5 -0.5

/1	Feb.27.1995	change		X.H	LM64C27P
	年月日 DATE	改定記事 REVISE	整理No	担当 PREPA	適用機種 MODEL

材質 MATERIAL	板厚 THICKNESS	仕上 FINSH	尺度 SCALE

名称 NAME	LCD UNIT OUTLINE DIMENSIONS
記号 SYMBOL	640XR·G·Bx480DOTS 1/240DUTY
部品コード PARTS CODE	

設計 DESIGN	書図 TRACE	照図 CHEC	検図 CHECK	承認 APPROVE	SHARP CORPORATION シャープ株式会社 液晶(事本)	作成日付 DATE	1994・09・14・
OHTSUCHI						図番 DRAWING No	